CODE	COURSE NAME	CATEGORY	L	T	P	CREDIT
222EEX102	EMBEDDED PROCESSOR DESIGN	INDUSTRY ELECTIVE	3	0	0	3

Preamble: This course aims to give an exposure to students on Processor-Pipelining, Memory organization, RISC-V Instruction Set Architecture and to create applications using Indigenous VEGA based Microcontroller.

Course Outcomes: After the completion of the course the student will be able to

CO 1	Apply the Instruction pipeline concept in IC design.
CO 2	Analyze the Hazards and Performance issues in Pipelining.
CO 3	Evaluate the Optimization techniques in Cache memory.
CO 4	Create IC designs using RISC-V Instruction set Architecture.
CO 5	Create an application using VEGA THEJAS32 Microcontroller.

Program Outcomes:

PO#	PO
PO 1	An ability to independently carry out research/investigation and development work in engineering and allied streams
PO 2	An ability to communicate effectively, write and present technical reports on complex engineering activities by interacting with the engineering fraternity and with society at large.
PO 3	An ability to demonstrate a degree of mastery over the area as per the specialization of the program. The mastery should be at a level higher than the requirements in the appropriate bachelor's program
PO 4	An ability to apply stream knowledge to design or develop solutions for real-world problems by following the standards
PO 5	An ability to identify, select and apply appropriate techniques, resources and state-of-the-art tools to model, analyze and solve practical engineering problems.
PO 6	An ability to engage in lifelong learning for the design and development related to the stream-related problems taking into consideration sustainability, societal, ethical and environmental aspects
PO 7	An ability to develop cognitive load management skills related to project management and finance which focus on Entrepreneurship and Industry relevance.

Mapping of course outcomes with program outcomes

	PO 1	PO 2	PO 3	PO 4	PO 5	PO 6	PO 7
CO 1	Y		Y	Y	Y	Y	
CO 2	Y		Y	Y	Y	Y	
CO 3	Y		Y	Y	Y	Y	
CO 4	Y		Y	Y	Y	Y	
CO 5	Y		Y	Y	Y	Y	

Assessment Pattern

Bloom's Category	End Semester Examination
Apply	40
Analyse	20
Evaluate	20
Create	20

Mark distribution

Total Marks	CIE	ESE	ESE Duration
100	40	60	2.5 hours

Continuous Internal Evaluation Pattern:

Continuous Internal Evaluation: 40 marks

Seminar/Data Collection & Interpretation/Quiz/Report based on Literature Survey on Recent Technology : 10 marks

Course based task/Micro project : 20 marks

Test paper 1 no. : 10 marks

Test paper shall include minimum 80% of the syllabus.

End Semester Examination Pattern:

End Semester Examination: 60 marks

The end semester examination will be conducted by the respective college.

There will be two parts; Part A and Part B.
Part A will contain 5 numerical/short answer questions with 1 question from each module, having 5 marks for each question (such questions shall be useful in the testing of knowledge, skills, comprehension, application, analysis, synthesis, evaluation and understanding of the students). Students should answer all questions.
Part B will contain 7 questions (such questions shall be useful in the testing of overall achievement and maturity of the students in a course, through long answer questions relating to theoretical/practical knowledge, derivations, problem solving and quantitative evaluation), with minimum one question from each module of which student should answer any five. Each question can carry 7 marks.

Model Question Paper

APJ ABDUL KALAM TECHNOLOGICAL UNIVERSITY
SECOND SEMESTER M.TECH DEGREE
EXAMINATION,OCT 2023
Branch: Electronics & Communication
Stream: EC5
***Course Code & Name:* 222EEX102 Embedded Processor Design**

	Answer *All Questions(5 Marks each)*
1.	Examine the performance evaluation methods in microprocessor architecture.
2.	Compare Structural hazards and Control Hazards.
3.	Distinguish Virtual and Physical cache.
4.	Examine the Control and Status Registers in RISC-V Architecture.
5.	Illustrate the Interrupt handling technique in VEGA THEJAS32 Microcontroller.
	Answer *Any 5 Questions(7 Marks each)*
6.	a)Differentiate between Computer Architecture and Organization (3 marks) b)Analyze different types of instructions in Computer organization (4 marks)
7	a)Examine the techniques of Static and Dynamic branch prediction(4 marks) b)Justify how to overcome the hazards in the pipeline(3 marks)
8.	a)Differentiate set associative and fully associative caches(4 marks) b)Illustrate Cache memory organization(3 marks)
9.	a)Examine the General-Purpose Registers in RISC-V Architecture(4 marks) b)Analyze operating modes of RISC-V ISA(3 marks)
10.	a)Illustrate design features of THEJAS32 Microcontroller (3 marks) b)Analyze Memory Mapped I/O in THEJAS32 Microcontroller(4 marks)
11.	a)Illustrate the basic and Advanced Optimization Techniques in Cache Memory(4 marks) b)Design a data path and control path of RISC-V ISA(3 marks)
12.	a)Differentiate data forwarding and data bypassing (3 marks) b)Illustrate different types of addressing modes in RISC-V ISA(4 marks)

Syllabus

Module 1 (8 Hours)

Introduction to computer Architecture: Basic Computer Organization, Performance Evaluation Methods, Introduction to RISC, Instruction Pipeline and Performance.

Module 2 (8 Hours)

Processor Pipelining: Basics of Pipelining, Classic five stage pipelining in RISC processor, Performance issues in pipelining, Pipeline Hazards (Structural hazards, Data Hazards, Control Hazards), Data forwarding and bypassing techniques, Branch prediction technique: Static and Dynamic branch prediction.

Module 3(8 Hours)

Memory hierarchy: Memory hierarchy, Locality of References, Cache memory principles, Types of caches (Virtual and Physical cache), Cache architecture, Direct mapped, set associative and fully associative caches, Block Replacement Techniques and Write Strategy, Design Concepts in Cache Memory. Basic and Advanced Optimization Techniques in Cache Memory.

Module 4(8 Hours)

RISC-V Architecture : RISC-V Instruction Set Architecture, Registers – General Purpose Registers, Control and Status Registers, Operating Modes, Programmers' Model for Base Integer ISA, Base Instruction Formats, Exceptions, Traps, and Interrupts, Machine-Level CSRs misa, mhartid, mstatus, mtvec medeleg and mideleg, mip and mie, mepc, mcause, mtval.

Module 5(8 Hours)

VEGA THEJAS32 Microcontroller: Functional Bock diagram, CPU, Memory Mapped input output and Interrupts Project using ARIES Development board.

Course Plan

No	Topic	No. of Lectures
1	**Introduction to computer Architecture:**	
1.1	Basic Computer Organization	2
1.2	Performance Evaluation Methods	2
1.3	Introduction to RISC Instruction Pipeline and Performance	4
2	**Processor Pipelining:**	
2.1	Basics of Pipelining	1
2.2	Classic five stage pipelining in RISC processor	1
2.3	Performance issues in pipelining	1
2.4	Pipeline Hazards (Structural hazards, Data Hazards, Control Hazards)	2
2.5	Data forwarding and bypassing techniques	1
2.6	Branch prediction technique: Static and Dynamic branch prediction.	2
3	**Memory hierarchy:**	

3.1	Memory hierarchy, Locality of References	1
3.2	Cache memory principles	1
3.3	Types of caches (Virtual and Physical cache)	1
3.4	Cache architecture	1
3.5	Direct mapped, set associative and fully associative caches	1
3.6	Block Replacement Techniques and Write Strategy	1
3.7	Design Concepts in Cache Memory	1
3.8	Basic and Advanced Optimization Techniques in Cache Memory	1
4	**RISC-V Architecture :**	
4.1	RISC-V Instruction Set Architecture	1
4.2	Registers – General Purpose Registers, Control and Status Registers	1
4.3	Operating Modes	1
4.4	Programmers' Model for Base Integer ISA	1
4.5	Base Instruction Formats	1
4.6	Exceptions, Traps, and Interrupts	1
4.7	Machine-Level CSRs misa, mhartid, mstatus, mtvec medeleg and mideleg, mip and mie, mepc, mcause, mtval.	2
5	**VEGA THEJAS32 Microcontroller:**	
5.1	Functional Bock diagram	1
5.2	CPU, Memory Mapped input output and Interrupts	2
5.3	Project using ARIES Development board	5

Reference

1. The RISC-V Reader by David A Patterson and Andrew Waterman First Edition
2. The RISC-V Instruction Set Manual Volume I: User-Level ISA Version 2.1
3. Computer Architecture, A quantitative approach by John L Hennessy and David A Patterson Fifth Edition
4. Computer organization and architecture, designing for performance, William Stallings Eight Edition
5. Georg Hager, Gerhard Wellein, Introduction to High Performance Computing for Scientists and Engineers, Chapman & Hall / CRC Computational Science series, 2011.